The Prototype of Real-Time Image Pre-Processing System for Satellites’ Remote Sensing

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Outline

- Motivation
- Architecture of CIS Integration Chip
- Results of CIS integration chip
- Image Demonstration
- Conclusions
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Motivation

- Satellite image: CCD or CIS
- The advantages of CIS:
  - Lower power consumption
  - CMOS comparable process
- Evaluate and setup the CIS technology for satellite usage in NARL.

Source: web, google
Motivation

- Cost is very high to realize 12000 pixels in single chip
  - Pixel size=6.5um, 12000 pixels~80mm

- Package 4 chips to realize the 2800pixels
Motivation

- Demo with CIS Chips
- LCD monitor shows the satellites’ image, which sources from Google Earth

Demo system setup
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The architecture of proposed real-time image pre-processing system for satellites’ remote sensing.
**Architecture of CIS & ICAI Chips**

- **CIS chip is composed of:**
  - TDP (Timing Data Processing)
  - Sensor
  - Level shifter
  - ADC (Analog-to-Digital Converter)

- **ICAI chip**
  - CIS control logic
  - Image combiner
  - SRAM
  - Host interface

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**Overall CIS system structure**

- CIS Chip
  - ICAI Chip
  - Host Computer

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**Diagram Details:**

- **Sensing area**
- **Timing Data Processing**
- **AFE**
- **Sensor**
- **clk**
- **DATA**
- **Interface**
- **(level shifter & ADC)**

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**CISD – Successful Platform Provider**
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CIS Chip

- CIS chip is composed of:
  - TDP (Timing Data Processing)
  - Sensor
  - Level shifter
  - ADC (Analog-to-Digital Converter)

- 0.18um technology (1P3M)

Overall CIS system structure
Sensor of CIS chip

- **Sensor**
  - pixel
  - read-out circuit

- **Pixel structure**
  - 3T
  - 4T
Sensor Layout

3T-2008

4T-2008

4T-2009

SW

VDD

RESET

MR

FD

TX

MX

pPD

p+ p-Si n+
- Higher sensitivity in 4T pixel
- Lower dark signal in 4T pixel
Sensor Linearity

- 4T linear range is smaller than 3T linear range
- Linearity affect color levels
- Increase linearity

![Graph showing sensor linearity](image-url)

- Output Voltage (mV) vs. Illumination (lx*ms)
- Sensitivity comparison between 3T_2008, 4T_2008, and 4T_2009
Measurement Result of Sensor -II

- Measurement results with light of different wavelength
- Measurement of test chips

![Graph showing voltage (mV) vs. power (mW/cm²) for blue, green, and red light.](image)
Refine the test setting.

**Dark Signal 4T**

- **Output Voltage (mV)** vs **Integration Time (mS)**

  - **rst=3v(mv)**
  - **rst=2.2v(mv)**

- **6.17mV/ms**
- **0.54mV/ms**

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CIS 4T Pixel Revision

- CIS 4T pixel (2009)
  - Shrink the gate size of TX
  - Increase a ladder between PD and TX

3T-2008

4T-2008

4T-2009
CIS 4T Pixel Results

- 4T CIS cell (2009 vs. 2008)
  - Sensitivity: 2.32x (3V)
  - Dark current: 1.28x (3V)

Vout vs. (Lux*mS)

Vout vs. integration time
Measurement Result of Sensor -IV

- Measurement of fixed pattern noise
- Measurement on full chip

![Graph showing fixed pattern noise measurement]

- 4T_fixed pattern noise
  +1.96%, -3.52%
Sensor-readout circuit

- Linearity of 99.82% with Correlated-Double-Sampling (CDS) readout circuit

CDS readout circuit

Simulated linearity of readout circuit

\[ R^2 = 0.9982 \]
- **Timing control logic of CIS chip**
- **Controls timing of exposure and image storage of CMOS image sensor array**

The diagram illustrates the circuit structure of TDP with labels for various components:

- Sensing area
- Sensor
- AFE (level shifter & ADC)
- Interface (I²C)
- Timing Data Pre-processing
- CIS chip

The chart includes labels for circuit elements such as:

- Mod-1000 Counter
- clamp_sel_bus logic
- cm_sel_bus logic
- col_sel_bus logic
- reset logic
- shr logic
- shs logic

The full CIS chip and the circuit structure of TDP are also shown in the image.
Simulation Result of TDP

- Simulation results: normal
- Function will be tested with CIS full chip

layout

col_sel_bus[703:0]  clamp_sel_bus[703:0]
Level shifter of CIS Chip

- Transform single-ended signal into fully-differential signal of desired common-mode level

role of level shifter in CIS system
Simulation Result of Level Shifter

- Switched-capacitor circuit
- Simulation results: normal
PGA & ADC of CIS Chip

- Convert analog signal of sensor into digital form for digital processing of ICAI chip

**Diagram:**
- Sensing area
  - Sensor
  - Timing
  - Data Pre-processing
  - AFE
  - level shifter & ADC
- Interface (I2C)
- clk
- DATA
- CIS chip

**Role of ADC in CIS System:**

```
Sensor + ROIC  ➔  Level Shifter ➔  PGA ➔  ADC ➔  CPU
```

```
PGA & ADC of CIS Chip
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The ENOB of cyclic ADC is 8.3 bit, which meets the spec. (8 bit)

- ENOB > 8 and SNDR > 50 dB within signal bandwidth
- Control clock from build-in TDP
- Static and dynamic performance meet requirement specified

### Measurement Results of PGA & ADC

<table>
<thead>
<tr>
<th>ADC Type</th>
<th>Fs (MS/s)</th>
<th>Fin (MHz)</th>
<th>SNDR (dB)</th>
<th>ENOB (bits)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cyclic ADC</td>
<td>10</td>
<td>1</td>
<td>63.0530</td>
<td>10.1816</td>
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<tr>
<td></td>
<td></td>
<td>5</td>
<td>60.9477</td>
<td>9.8318</td>
</tr>
</tbody>
</table>

**post-simulation result**

![Circuit Diagram](image)

- measured INL/DNL
- ENOB V.S. input frequency
4 CIS Chips in a Package

- System Block include mother board and system package

Chip Layout

CIS x 4

System Package

Voltage Bias & Current Bias

Mother Board

To 2'nd Gen. Embedded System

System Block

Package

Chip

Chip

Chip

Chip

Chip

System Block

4 CIS Chips in a Package

• System Block include mother board and system package
Confirm the Performance of 4 CIS Chips

- Partial exposure to confirm the quality of 2800 pixels.

**Full exposure**

**Partial exposure**
· ICAI (Image Combiner and Acquisition Interface)
· 0.18um Technology
· ICAI chip was successfully fabricated and functional.

ICAI chip
Summary of Measurement Results

- **Sensor**: met spec. except
  - dark signal (improvement needed)
  - temporal noise which cannot be measured with current measurement environment
- **Level shifter**: OK
- **TDP**: OK
- **ADC**: OK
- **CIS full chip**: OK (verified by demonstration)
- **ICAI**: OK
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Demo System Setup

- Establishment of demo system had been completed
- Demo software (Tellurion) & FPGA board (DE2-70) are synchronized with RS232 driver
- Demo with CIS Chip

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demo system

CIS Mother Board

- CIS and Lens
- Demo Software
- CMOS Image Sensor Array (mother board & single Chip)
- DC 5V
- DC 9V
- Display
- VGA
- Client PC
- RS-232 Driver
- FPGA
- GPIO Driver
- ICAI
- Frame Buffer
- Host (DE-2 70 Development Kit)

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CISD–Successful Platform Provider
Demonstration Result (single chip)

- Successfully demonstrate the image by the integration chip.
Demonstration System Improvement

- Setup a tunable z-axis demonstration holder in 2010
Demo System Setup (4 Chips)

- PGA in PCB
Demo System Setup (4 Chips)

- Demo software (Tellurion) & FPGA board (DE2-70) are synchronized with RS232 driver

CIS Chip and Lens

4 Chip demo system
Demonstration System

Overview

Lens and holder
CIS integration chip performance

- Image with single chip (700 pixels)
- Images are not clear enough
Image Comparison (v.1 vs. v.2)

- Much higher resolution (2800 pixels/strip)
- Higher contrast
- More accurate focus
Demonstration Result

- Resolution is 2800 Pixel
- Test with resolution chart
- White point can be solved by adjusting bandwidth of DRAM on FPGA board
Demonstration Result
Demonstration

Industrial District
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Conclusions

- Successfully demonstrate the image by 4 chips in package (2800 pixels)
- CIS pixel
  - 4T pixel was chose
  - Linearity and dark current improvement
  - TDI study
- Image improvement
- Future works
  - FPGA function realized by chip
  - 4 CIS and ICAI chips in the same board
Real-time Image Pre-processing SoC

- Completed the FPGA based prototype verification
- Starts the integration and verification of subcircuits
Acknowledgement

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Thanks for Your Attention!